

Day : Friday  
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# PALM INTRANET

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## Inventor Name Search Result

Your Search was:

Last Name = MOLL

First Name = LAURENT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">11543549</a>	Not Issued	41	10/04/2006	Cache instructions with hierarchy control	MOLL, LAURENT R.
<a href="#">11543598</a>	Not Issued	94	10/04/2006	CACHE OPERATIONS WITH HIERARCHY CONTROL	MOLL, LAURENT R.
<a href="#">11559069</a>	Not Issued	30	11/13/2006	SMALL AND POWER-EFFICIENT CACHE THAT CAN PROVIDE DATA FOR BACKGROUND DMA DEVICES WHILE THE PROCESSOR IS IN A LOW-POWER STATE	MOLL, LAURENT R.
<a href="#">11559133</a>	Not Issued	30	11/13/2006	POWER CONSERVATION VIA DRAM ACCESS REDUCTION	MOLL, LAURENT R.
<a href="#">11559192</a>	Not Issued	20	11/13/2006	POWER CONSERVATION VIA DRAM ACCESS	MOLL, LAURENT R.
<a href="#">11717511</a>	<a href="#">7424561</a>	150	03/13/2007	SYSTEMS USING MIX OF PACKET, COHERENT, AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS	MOLL, LAURENT R.
<a href="#">11740892</a>	<a href="#">7443759</a>	150	04/26/2007	REDUCED-POWER MEMORY WITH PER-SECTOR GROUND CONTROL	MOLL, LAURENT R.
<a href="#">11740901</a>	Not Issued	30	04/26/2007	Reduced-Power Memory with Per-Sector Power/Ground Control and Early Address	MOLL, LAURENT R.
<a href="#">11751949</a>	Not Issued	30	05/22/2007	RE-FETCHING CACHE MEMORY ENABLING LOW-POWER MODES	MOLL, LAURENT R.
<a href="#">11751973</a>	Not Issued	30	05/22/2007	RE-FETCHING CACHE MEMORY ENABLING ALTERNATIVE OPERATIONAL MODES	MOLL, LAURENT R.
<a href="#">11751985</a>	Not Issued	30	05/22/2007	RE-FETCHING CACHE MEMORY HAVING COHERENT RE-FETCHING	MOLL, LAURENT R.
<a href="#">11759216</a>	Not Issued	25	06/06/2007	Software-Directed Rank Coalescing	MOLL, LAURENT R.

<a href="#">11759217</a>	Not Issued	30	06/06/2007	Physical Memory Allocating According to Ranks	MOLL, LAURENT R.
<a href="#">11759218</a>	Not Issued	30	06/06/2007	Associative Structure Rank Counters	MOLL, LAURENT R.
<a href="#">11803637</a>	Not Issued	30	05/15/2007	Systems including packet interfaces, switches, and packet DMA circuits for splitting and merging packet streams	MOLL, LAURENT R.
<a href="#">11933297</a>	Not Issued	25	10/31/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT R.
<a href="#">11933319</a>	Not Issued	25	10/31/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT R.
<a href="#">11933333</a>	Not Issued	30	10/31/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT R.
<a href="#">12362679</a>	Not Issued	25	01/30/2009	Hypertransport/SPI-4 Interface Supporting Configurable Deskewing	MOLL, LAURENT R.
<a href="#">60731784</a>	Not Issued	159	10/31/2005	Extend cache operations to provide control over which levels of the hierarchy they apply to	MOLL, LAURENT R.
<a href="#">60731969</a>	Not Issued	159	10/31/2005	Instructions giving hints to the hardware prefetcher for more efficient prediction of prefetches	MOLL, LAURENT R.
<a href="#">60736632</a>	Not Issued	159	11/15/2005	Power conservation via DRAM access reduction	MOLL, LAURENT R.
<a href="#">60736736</a>	Not Issued	159	11/15/2005	Small and power-efficient cache that can provide data for background DMA devices while the processor is in a low-power state	MOLL, LAURENT R.
<a href="#">60743560</a>	Not Issued	159	03/20/2006	Prefetch Hardware Efficiency via Prefetch Hint Instructions	MOLL, LAURENT R.
<a href="#">60744592</a>	Not Issued	159	04/10/2006	Improved Prefetch Hardware Efficiency via Prefetch Hint Instructions	MOLL, LAURENT R.
<a href="#">60746049</a>	Not Issued	159	04/30/2006	Reduced Power Cache Memory With Per-Sector Power Control	MOLL, LAURENT R.
<a href="#">60747200</a>	Not Issued	159	05/14/2006	Reduced Power Cache Memory With Per-Sector Power Control	MOLL, LAURENT R.
<a href="#">60747818</a>	Not Issued	159	05/22/2006	Re-Fetching Cache Memory	MOLL, LAURENT R.
<a href="#">60761220</a>	Not Issued	159	01/23/2006	Power conservation via DRAM access reduction	MOLL, LAURENT R.
<a href="#">60761925</a>	Not Issued	159	01/25/2006	Small and power-efficient cache that can provide data for background DMA devices while the processor is in a low-power state	MOLL, LAURENT R.

<a href="#">60803367</a>	Not Issued	159	05/28/2006	Re-fetching Cache Memory	MOLL, LAURENT R.
<a href="#">60804085</a>	Not Issued	159	06/06/2006	Application-Directed Rank Coalescing for Memory Power Management	MOLL, LAURENT R.
<a href="#">09517369</a>	<a href="#">6314156</a>	150	03/02/2000	Space-efficient multi-cycle barrel shifter circuit	MOLL, LAURENT RENE
<a href="#">10821397</a>	<a href="#">7240141</a>	150	04/09/2004	PROGRAMMABLE INTER-VIRTUAL CHANNEL AND INTRA-VIRTUAL CHANNEL INSTRUCTIONS ISSUING RULES FOR AN I/O BUS OF A SYSTEM-ON-A-CHIP PROCESSOR	MOLL, LAURENT RENE
<a href="#">60380740</a>	Not Issued	159	05/15/2002	System on chip for networking	MOLL, LAURENT RENE
<a href="#">09114753</a>	<a href="#">6292762</a>	150	07/13/1998	METHOD FOR DETERMINING A RANDOM PERMUTATION OF VARIABLES BY APPLYING A TEST FUNCTION	MOLL, LAURENT RENE
<a href="#">09763724</a>	<a href="#">6844424</a>	150	02/27/2001	METHOD FOR OBTAINING AVIAN BIOLOGICAL PRODUCTS	MOLLARD, LAURENT
<a href="#">11111886</a>	Not Issued	93	04/22/2005	MOULD FOR NANO-PRINTING, PROCESS FOR MANUFACTURING SUCH A MOULD AND USE OF SUCH A MOULD	MOLLARD, LAURENT
<a href="#">10395505</a>	<a href="#">7275216</a>	150	03/24/2003	SYSTEM AND METHOD FOR DESIGNING ELECTRONIC FORMS AND HIERARCHICAL SCHEMAS	MOLLICONE, LAURENT
<a href="#">10395506</a>	<a href="#">7415672</a>	150	03/24/2003	SYSTEM AND METHOD FOR DESIGNING ELECTRONIC FORMS	MOLLICONE, LAURENT
<a href="#">10459179</a>	<a href="#">7168035</a>	150	06/11/2003	BUILDING A VIEW ON MARKUP LANGUAGE DATA THROUGH A SET OF COMPONENTS	MOLLICONE, LAURENT
<a href="#">10632437</a>	Not Issued	71	08/01/2003	Conversion of structured documents	MOLLICONE, LAURENT
<a href="#">10854961</a>	<a href="#">7281018</a>	150	05/26/2004	FORM TEMPLATE DATA SOURCE CHANGE	MOLLICONE, LAURENT
<a href="#">11072087</a>	Not Issued	71	03/04/2005	Designer-created aspect for an electronic form template	MOLLICONE, LAURENT
<a href="#">11107347</a>	Not Issued	61	04/15/2005	Query to an electronic form	MOLLICONE, LAURENT
<a href="#">11203818</a>	Not Issued	61	08/15/2005	Recognizing data conforming to a rule	MOLLICONE, LAURENT

<a href="#">11320208</a>	<a href="#">7505994</a>	150	12/28/2005	XPATH EXPRESSION BINDING USING XPATH TRACKER WITH DYNAMIC OR STATIC PATH EVALUATION	MOLLICONE, LAURENT
<a href="#">11567133</a>	Not Issued	30	12/05/2006	Building Electronic Forms	MOLLICONE, LAURENT
<a href="#">11567140</a>	Not Issued	30	12/05/2006	Incrementally Designing Electronic Forms and Hierarchical Schemas	MOLLICONE, LAURENT
<a href="#">11567149</a>	Not Issued	30	12/05/2006	Closer Interface for Designing Electronic Forms and Hierarchical Schemas	MOLLICONE, LAURENT

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